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CTI Project

The second generation digital video transmission standard for terrestrial application (DVB-T2) has been designed at the same time as the second generation cable video standard DVB-C2 and they share many building blocks. Hence, a receiver capable of decoding both DVB-T2 and DVB-C2 signals (multi-standard receiver) is a relevant example of reconfigurable device, where processing blocks are reconfigured according to the considered transmission format. This project aims at providing a study on an Integrated Terrestrial And CAble Receiver Design (ITACA-RD) and will leverage on the knowledge of the DVB-T2 receiver acquired by the previous CTI project on *DVBT2 advanced software platform* (DASP) carried out by the same partners.
The multi standard device will be a home receiver, able to decode both the DVB-T2 signal coming from the rooftop antenna and the DVB-C2 signal coming from the cable. We will first compare the two standards, identifying common and different blocks, then the critical parts of the DVB-C2 receiver will be investigated proposing suitable algorithms providing the intended trade-off between performance and implementation complexity. Particular attention will be paid to synchronization, channel estimation, demapping and the impact of impairments on the integrated receiver, that will provide guidelines for future design of the front-end. The outcome of the project will be, beyond design guidelines for a chip implementation, an Octave simulator of the multi standard receiver.
The simulator will integrate the blocks developed within the DASP project for the DVB-T2 standard. A preliminary evaluation of the expected performance in a comparison with existing available data will be also performed.

Main Objectives

The ITACA-RD has the following main objectives:

1. an in depth study of an architecture for an integrated implementation of a multi standard receiver,
2. an in depth study of synchronization, which is the critical part of the C2 receiver,
3. an in depth study of the channel estimation for both standards,
4. an in depth study of the Forward Error Correction Decoder (FEC Decoder), especially focusing on demapping process, with the aim of providing guidelines for an effective implementation on a chip,

Objective 1:

There are not open position for this task.

Objective 2: Synchronization

C2 and T2 provide different synchronization procedures corresponding to different modulation techniques. This is why the synchronization proposed in the DASP project has to be reviewed and the synchronization structure redesigned to be compatible with both standards. Here we summarize the main issues in the synchronization of the C2 system.

Synchronization for C2

The framing structure of C2 is reported in Fig. 1. Each frame comprises a preamble and data blocks. The preamble is built with a number of signalling L1 blocks are transmitted with regular carrier spacing of 7.61 MHz (. The preamble consists of a frequency cyclic repetition of the L1 blocks, that are repeated every 7.61MHz. The highest frequency of each L1 block is a multiple of a 7.61 MHz, however the spectrum of the data of the C2 signal may start and end in any position of the spectrum. Each L1 block includes 32 OFDM symbols that contain signalling information. The cells of the L1 OFDM symbols laying outside the data

spectrum are not transmitted, according to what is known as *absolute OFDM* system [8]. Pilots within these OFDM symbols can be exploited to obtain synchronization.

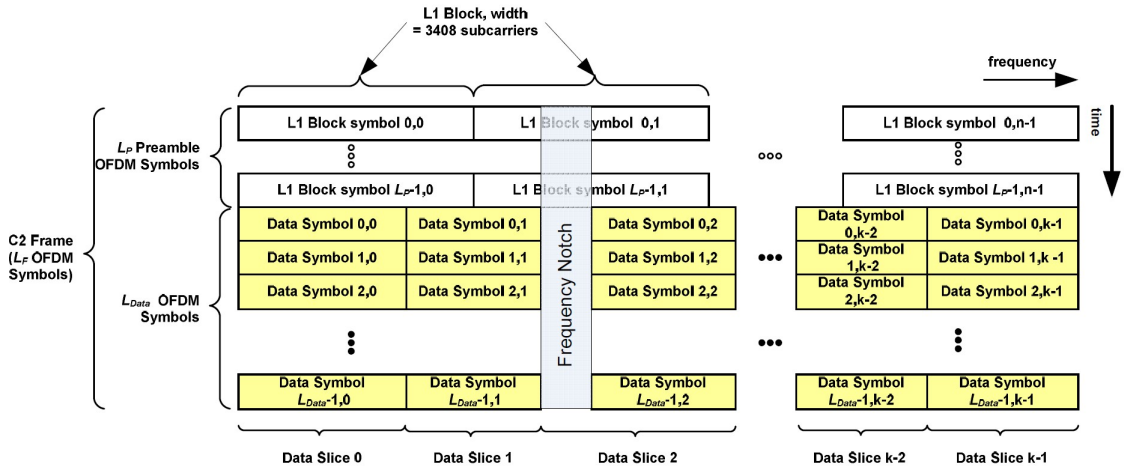

Fig. 1 Frame Structure

As can be seen from Fig. 1, data bits are organized in *data slices* that do not occupy a predetermined bandwidth. Each data slice is generated using an 4K OFDM modulator and this set the maximum number of carriers available for a data slice to 3408. In order to generate data slices that occupy a smaller band than the maximum 8 MHz bandwidth, some cells of each OFDM symbol are kept empty (i.e. no transmission occurs on these cells). In order to have an efficient use of the spectrum, the frequencies where these empty cells are located can be used by another data slice: this is obtained by adjusting the carrier frequency of the transmission of each data slice. In other words, while in T2 the carriers of adjacent (in the frequency domain) channels are spaced by a fixed amount (e.g. 8 MHz), in C2 the spacing between channel carrier frequencies is not fixed but can be adjusted according to the needs of each data slice. This packing of data slices in the spectrum comes also under the name of *channel bundling.* A receiver interested to decode only one data slice can extract the part of the broader transmission signal that contains the required service, according to the *segmented OFDM reception* [11]. In order to reduce interference with other existing wireless communication systems, notches can be introduced in the C2 signal, obtained by setting to zero some sub-carriers of the OFDM signal.

The project will investigate how to implement synchronization ensuring a fast and reliable procedure, able to work also in adverse channel conditions. The spectrum detection is new with respect to T2 standard. In fact, although guard interval detection was already present in T2, the absence of the P1-symbol and the short size of the OFDM symbol will require more efficient synchronization techniques.
Lastly, the pilot-based frequency synchronization is different from what is provided in T2 and therefore will require a special design by itself. Moreover, since differential binary shift keying (DBSSK) is adopted in the C2 preamble, the frequency synchronization will operate across OFDM symbols exploiting the feature of the differential modulation.

Objective 3: Channel Estimation

Both T2 and C2 standards provide pilot cells within the OFDM symbols that contain symbols known at the receiver and can be used to perform channel estimation. The C2 standard provides a sub-set of the set of pilot patters of T2, i.e. the allocation of cells used to transmit the training and their content. This is due to the different channels over which transmission occurs: while for T2 we have high delay spread and potential Doppler spreads, the C2 channels have a shorter durations and the variations over time are mainly due to residual synchronization errors. As a consequence, pilot patterns in C2 are only the sparser patterns of T2.

The C2 operates at high signal to noise ratio and with less dispersive/time varying channels more accurate channel estimators may be needed in order to reduce the impact of estimation error on the overall performance. For example, in the presence of perfect channel estimation, the required signal to noise ratios to achieve a bit error rate of 10-4 at the output of the LDPC decoder are up to 22 dB for T2 [9] and up to 35 dB for C2 [8] on an AWGN channel.

Indeed, the estimation process provides interpolators that are sub-optimal for the sake of a simpler implementation and that provide negligible errors for T2. However, in a higher signal to noise ratio environment these errors may become relevant. On the other hand, since the channel in C2 is less time-varying than for T2, we can improve the performance of the estimator by longer time-interpolators that would otherwise be useless in T2.

The main of this project is to study channel estimation techniques for C2. The channel estimation is typically implemented in three steps: Raw Estimation, Refinement Filtering and Interpolation. This part will focus on each of these three parts, providing algorithms for each of them.

Another important aspect of the channel estimation is the noise estimation. The noise power estimation has a significant impact on FEC Decoding Process. This is why, one of the objective is to study algorithms to estimate noise power level.

Both estimators, for channel and noise level, will be integrated in the simulator, and their performances will be evaluated in the using the receiver simulation chain.

Objective 4: FEC Decoding Algorithms: Demapper and LPDC Decoder

The FEC Decoding Algorithms, taken into account by this part of the project, will be the Demapping and the LDPD Decoding.

Demapper

The demapper is a component of the demodulator that generates the log-likelihood ratios on the data bits starting from the received signal. Various solutions for the demapper of the T2 receiver have already been developed and indeed it has been verified that the desired trade-off between complexity and performance is challenging for the considered scenario.
We expect that C2 will pose even higher challenges, since this standards provides higher order QAM constellations (up to 4096-QAM versus the 256-QAM of T2) and the required signal to noise ratio is increased. In particular, the demapper shall be able to generate log likelihood ratios of up to 12 bits per symbol starting from received samples quantized with smaller step sizes than that of the T2 receiver in order to be suited to denser constellations and higher signal to noise ratios.

C2 and T2 do not use the same modulations. The C2 provides high order QAM constellations (up to 4096-QAM) while the novelty of the T2 is the use of the rotated constellation. An exhaustive demapping process, for the 4096-QAM, is too complex to be suitable for a real implementation. This is why we will focus on low computation solutions and on sub-optimal algorithms for the demapping process. Few different algorithms will be proposed and evaluated in terms of complexity end performance. The performance will be evaluated by simulations while the complexity will be analyzed in terms of number of operations per samples. The goal is to identify an algorithm suitable for implementation and to propose a common architecture able to process 4096-QAM and rotated constellation.

LDPC Decoder

There are not open position for this task.